CLAIM LISTING

No claims have been amended, canceled, or added. A Claim Listing is provide as a courtesy.

1. (Previously Presented) A method, comprising:

allocating an original percentage of bandwidth or number of accesses tc memory by a memory controller; and

increasing the bandwidth or number of accesses allocated to the n emory controller to a percentage higher than the original percentage of bandwidth or nun ber of accesses allocated when accesses to memory by the memory controller is less tl an the original percentage of bandwidth or number of accesses allocated to the memory con roller; and

decreasing the bandwidth or number of accesses allocated to the n emory controller to a percentage lower than an original bandwidth or number of accesses al ocated when accesses to memory by the memory controller are more than the original percen age of bandwidth or number of accesses allocated to the memory controller.

2. (Original) The method of claim 1, further comprising:

setting a window of time to monitor the percentage of bandwidth or nun ber of accesses to memory by the memory controller; and

measuring the percentage of bandwidth used or number of accesses to memory by the memory controller during the window of time.

3. (Original) The method of claim 1, further comprising applying a mask to increa e the bandwidth or number of accesses allocated to the memory controller to a percentage hi her than the original percentage of bandwidth or number of accesses allocated when acces s to memory by the memory controller are less than the original percentage of bandwidth o number of accesses allocated to the memory controller.

4. (Original) The method of claim 1, further comprising applying a mask to decre se the

bandwidth or number of accesses allocated to the memory controller to a percentage l(wer than an original bandwidth or number of accesses allocated when accesses to memory)y the memory controller are less than the original percentage of bandwidth or number of acc :sses allocated to the memory controller.

5. (Previously Presented) An article of manufacture article of manufacture, comp ising:

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the operations comprising,

allocating an original percentage of bandwidth or number of acc :sses to memory by a memory controller;

increasing the bandwidth or number of accesses allocated to the memory controller to a percentage higher than the original percentage of bandwidth or number of accesses allocated when accesses to memory by the memory controller are l :ss than the original percentage of bandwidth or number of accesses allocated to the mem(ry controller; and

decreasing the bandwidth or number of accesses allocated to the memory controller to a percentage lower than an original bandwidth or number of acce :ses allocated when accesses to memory by the memory controller are more than the origin: l percentage of bandwidth or number of accesses allocated to the memory controller.

6. (Original) The article of manufacture of claim 5, wherein the machine-acc :ssible medium further includes data that cause the machine to perform operations comprising

setting a window of time to monitor the percentage of bandwidth or nun ber of accesses to memory by the memory controller; and

measuring the percentage of bandwidth used or number of accesses to memory by the memory controller during the window of time.

7. (Original) The article of manufacture of claim 5, wherein the machine-accessib :e medium further includes data that cause the machine to perform operations comprising applying a mask to increase the bandwidth or number of accesses allocated to the mem)ry controller to a percentage higher than the original percentage of bandwidth or number (f

accesses allocated when accesses to memory by the memory controller are less than th : original percentage of bandwidth or number of accesses allocated to the memory conu)ller.

8. (Original) The article of manufacture of claim 5, wherein the machine-accessit e medium further includes data that cause the machine to perform operations comprisin applying a mask to decrease the bandwidth or number of accesses allocated to the men ory controller to a percentage lower than an original bandwidth or number of accesses allo ated when accesses to memory by the memory controller are less than the original percenta e of bandwidth or number of accesses allocated to the memory controller.

9. (Previously Presented) An apparatus, comprising:

a chipset having:

a processor having an original percentage of memory bandwidth or number of memory accesses allocated to it; and

a memory controller to increase the percentage of memory band vidth or the number of memory accesses allocated to the processor when the actual percenta e of bandwidth or number of accesses to the memory by the processor is less than the origi al percentage of bandwidth or number of accesses allocated to the processor, the memory controller further to decrease the percentage of memory bandwidth or the number of m mory accesses allocated to the processor when the actual percentage of bandwidth or numbe of memory accesses by the processor is more than the original percentage of memory bandwidth or number of memory accesses allocated to the processor.

10. (Previously Presented) The apparatus of claim 9, further comprising:

a first register in the memory controller to set the percentage of memory bandwidth or the number of memory accesses allocated to the processor;

a second register in the memory controller to set a window of time to m nitor percentage of memory bandwidth or number of memory accesses used by the processo ; and

a counter in the memory controller to measure percentage of memory bandwidth used or number of memory accesses by the processor during the window of ime.

11. (Previously Presented) The apparatus of claim 10, wherein the memory contro er further comprises a mask to increase the percentage of memory bandwidth or the num er of memory accesses allocated to the processor when memory accesses by the processor i: less than the percentage of memory bandwidth or the number of memory accesses allocate to the processor.

12. (Previously Presented) The apparatus of claim 10, wherein the memory control er further comprises a mask to decrease the percentage of memory bandwidth or the num er of memory accesses allocated to the processor when memory accesses by the processor is more than the percentage of memory bandwidth or the number of memory accesses allocate to the processor.

13. (Previously Presented) The apparatus of claim 9, wherein the chipset further comprises:

a graphics memory having an original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to it; and

a graphics controller to increase the percentage of graphics memory bandwidth or the number of graphics memory accesses allocated to the graphics memo y when the actual percentage of graphics memory bandwidth or number of graphics men ory accesses is less than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the graphics memory, the graphics controller fu ther to decrease the percentage of graphics memory bandwidth or the number of graphics m mory accesses allocated to the graphics memory when the actual percentage of graphics men ory bandwidth or number of graphics memory accesses is more than the original percentag of graphics memory bandwidth or number of graphics memory accesses allocated to the graphics memory.

14. (Previously Presented) The apparatus of claim 13, wherein the chipset further comprises one or more input/output (I/O) devices, an individual I/O device having an o iginal percentage of graphics memory bandwidth or number of graphics memory accesses all cated to it, the graphics controller to increase the percentage of graphics memory bandwidth r the

number of graphics memory accesses allocated to the one or more I/O devices when tl e actual percentage of graphics memory bandwidth or number of graphics memory acce sses is less than the original percentage of graphics memory bandwidth or number of graphic: memory accesses allocated to the one or more I/O devices, the graphics controller furt er to decrease the percentage of graphics memory bandwidth or the number of graphics me ıory accesses allocated to the one or more I/O devices when the actual percentage of graph :s memory bandwidth or number of graphics memory accesses is more than the original percentage of graphics memory bandwidth or number of graphics memory accesses all ›cated to the one or more I/O devices.

15. (Previously Presented) The apparatus of claim 13, wherein the processor furthe includes an original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to it, the graphics controller to increase the percentage of g aphics memory bandwidth or the number of graphics memory accesses allocated to the proce: ›or when the actual percentage of graphics memory bandwidth or number of graphics men ory accesses is less than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the processor, the graphics controller further to decrease the percentage of graphics memory bandwidth or the number of graphics mer ory accesses allocated to the processor when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is more than the original percentag : of graphics memory bandwidth or number of graphics memory accesses allocated to the processor.

16. (Previously Presented) The apparatus of claim 9, wherein the chipset further comprises a graphics memory having an original percentage of graphics memory band· ›idth or number of graphics memory accesses allocated to it, the graphics memory to increas : the percentage of graphics memory bandwidth or the number of graphics memory accesse: allocated to itself when an actual percentage of graphics memory bandwidth or numbe› of graphics memory accesses is less than the original percentage of graphics memory ban· width or number of graphics memory accesses allocated to itself, the graphics memory furthe to decrease the percentage of graphics memory bandwidth or the number of graphics men ory

accesses allocated to itself when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is more than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to itself.

17. (Previously Presented) The apparatus of claim 16, wherein the chipset further comprises one or more input/output (I/O) devices, an individual I/O device having an original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to it, the graphics memory to increase the percentage of graphics memory bandwidth or the number of graphics memory accesses allocated to the one or more I/O devices when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is less than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the one or more I/O devices, the graphics memory further to decrease the percentage of graphics memory bandwidth or the number of graphics memory accesses allocated to the one or more I/O devices when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is more than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the one or more I/O devices.

18. (Previously Presented) The apparatus of claim 16, wherein the processor further includes an original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to it, the graphics memory to increase the percentage of graphics memory bandwidth or the number of graphics memory accesses allocated to the processor when an actual percentage of graphics memory bandwidth or number of graphics memory accesses is less than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the processor, the graphics memory further to decrease the percentage of graphics memory bandwidth or the number of graphics memory accesses allocated to the processor when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is more than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the processor.

19. (Previously Presented) The apparatus of claim 9, wherein the chipset further comprises one or more input/output (I/O) devices having an original percentage of me ıory bandwidth or number of memory accesses allocated to it, wherein the memory control ɔr is to increase the percentage of memory bandwidth or the number of memory accesses allo ated to the one or more I/O devices when an actual percentage of memory bandwidth or nu ıber of memory accesses by the one or more I/O devices is less than the original percentag of memory bandwidth or number of memory accesses allocated to the one or more I/O de /ices, the memory controller further to decrease the percentage of memory bandwidth or the number of memory accesses allocated to the one or more I/O devices when the actual percentage of memory bandwidth or number of memory accesses by the one or more I O devices is more than the original percentage of memory bandwidth or number of mem ry accesses allocated to the one or more I/O devices.

20. (Previously Presented) An apparatus, comprising:

a processor having an original percentage of memory bandwidth or nun ɔer of memory accesses allocated to it, the processor having further a memory controller to ir ɔrease the percentage of memory bandwidth or the number of memory accesses allocated to tl e processor when the actual percentage of bandwidth or number of accesses to the mem y by the processor is less than the original percentage of bandwidth or number of accesses allocated to the processor, the memory controller further to decrease the percentage of memory bandwidth or the number of memory accesses allocated to the processor when the actual percentage of bandwidth or number of memory accesses by the processor is mo : than the original percentage of memory bandwidth or number of memory accesses allocated to the processor.

21. (Previously Presented) The apparatus of claim 20, further comprising:

a first register in the memory controller to set the percentage of memory bandwidth or the number of memory accesses allocated to the processor;

a second register in the memory controller to set a window of time to m nitor percentage of memory bandwidth or number of memory accesses used by the processo ; and

a counter in the memory controller to measure percentage of memory bandwidth used or number of memory accesses by the processor during the window of time.

22. (Previously Presented) The apparatus of claim 20, wherein the memory controller further comprises a mask to increase the percentage of memory bandwidth or the number of memory accesses allocated to the processor when memory accesses by the processor is less than the percentage of memory bandwidth or the number of memory accesses allocated to the processor.

23. (Previously Presented) The apparatus of claim 20, wherein the memory controller further comprises a mask to decrease the percentage of memory bandwidth or the number of memory accesses allocated to the processor when memory accesses by the processor is more than the percentage of memory bandwidth or the number of memory accesses allocated to the processor.

24. (Previously Presented) A method, comprising:

allocating to a processor an original percentage of memory bandwidth or number of memory accesses;

increasing the memory bandwidth or number of memory accesses allocated to the processor to a percentage higher than the original percentage of memory bandwidth or number of memory accesses allocated to the processor when actual accesses to memory by the processor is less than the original percentage of memory bandwidth or number of memory accesses allocated to the processor; and

decreasing the bandwidth or number of accesses allocated to the processor to a percentage lower than an original memory bandwidth or number of memory accesses allocated to the processor when actual accesses to memory by the memory controller are more than the original percentage of bandwidth or number of accesses allocated to the processor.

25. (Previously Presented) The method of claim 24, further comprising:

setting a window of time to monitor the percentage of bandwidth or number of

accesses to memory by the processor; and

measuring the percentage of bandwidth used or number of accesses to memory by the processor during the window of time.

26. (Previously Presented) The method of claim 25, further comprising applying a mask to increase the bandwidth or number of accesses allocated to the processor to a percentage higher than the original percentage of bandwidth or number of accesses allocated when accesses to memory by the processor are less than the original percentage of bandwidth or number of accesses allocated to the processor.

27. (Previously Presented) The method of claim 25, further comprising applying a mask to decrease the bandwidth or number of accesses allocated to the processor to a percentage lower than an original bandwidth or number of accesses allocated when accesses to memory by the processor are less than the original percentage of bandwidth or number of accesses allocated to the processor .

28. (Previously Presented) The apparatus of claim 24, further comprising:

allocating to a graphics controller an original percentage of memory bandwidth or number of memory accesses;

increasing the memory bandwidth or number of memory accesses allocated to the graphics controller to a percentage higher than the original percentage of memory bandwidth or number of memory accesses allocated to the graphics controller when actual accesses to memory by the graphics controller is less than the original percentage of memory bandwidth or number of memory accesses allocated to the graphics controller; and

decreasing the bandwidth or number of accesses allocated to the graphics controller to a percentage lower than an original memory bandwidth or number of memory accesses allocated to the graphics controller when actual accesses to memory by the memory controller are more than the original percentage of bandwidth or number of accesses allocated to the graphics controller.

29. (Previously Presented) The apparatus of claim 24, further comprising:

allocating to one or more input/output (I/O) devices an original percentage of memory bandwidth or number of memory accesses;

increasing the memory bandwidth or number of memory accesses allocated to the one or more I/O devices to a percentage higher than the original percentage of memory bandwidth or number of memory accesses allocated to the one or more I/O devices when actual accesses to memory by the one or more I/O devices is less than the original percentage of memory bandwidth or number of memory accesses allocated to the one or more I/O devices; and

decreasing the bandwidth or number of accesses allocated to the one or more I/O devices to a percentage lower than an original memory bandwidth or number of memory accesses allocated to the one or more I/O devices when actual accesses to memory by the memory controller are more than the original percentage of bandwidth or number of accesses allocated to the one or more I/O devices.